Amendments to the Disclosure

Please cancel paragraphs [0013]-[0014] currently on file and substitute therefor the following encoded paragraphs [0013]-[0014.2].

[0013] According to a first broad aspect of an embodiment of the present invention there is disclosed a method for collecting memory failure information in real time while performing a test of memory embedded in a circuit, comprising, for each column or row of a memory under test, the steps of: (a) successively conducting uninterrupted testing of each memory location of said column or row according to a memory test algorithm under control of a first clock; (b) selectively generating a failure summary on-circuit while continuing to perform said uninterrupted testing of each memory location of said column or row; and (c) transferring off-circuit said failure summary from said circuit under control of a second clock concurrently with uninterrupted testing of a next column or row in sequence.

[0014] According to a second broad aspect of an embodiment of the present invention there is disclosed a method of collecting memory failure information in real time while performing a test of memory embedded in a circuit for memory test phases that use a column or a row access mode, comprising, for each memory column or row under test: testing each memory location of said column or row according to a memory test algorithm under control of a first clock; generating on-circuit a failure summary while testing said column or row, said generating a failure summary including, for each detected failure; determining whether said detected failure is a massive failure or a non-massive failure; and, if said detected failure is a non-massive failure: classifying said detected failure according to predetermined failure types; and updating a failure mask register with results of comparisons of memory outputs and expected memory outputs; incrementing a count of each detected

failure type; and storing the row or column address of the first and last failures in said column or row, respectively; upon completion of testing of said column or row, selecting a failure summary data depending upon whether a column or row was tested; and transferring said failure summary from said circuit under control of said second clock concurrently with testing of the next column or row in sequence.

[0014.1] According to a third broad aspect of the embodiment of the present invention, there is disclosed a memory test controller for testing a memory in a circuit, comprising means for conducting testing of each memory location of a column or row of said memory according to a test algorithm under control of a first clock in uninterrupted fashion; means for generating a failure summary while testing the column or row of said memory; and means for transferring said failure summary from said circuit via a circuit output under control of a second clock while testing a next column or rows if any, of a memory under test.

[0014.2] According to a fourth broad aspect of an embodiment of the present invention, there is disclosed a memory test controller for testing memory in a circuit, comprising: means for testing each memory location of a column or row of a memory under test according to a test algorithm under control of a first clock; a failure summary generator for generating a failure summary while testing a column or row of said memory, including: failure type identification means responsive to a failure mask for classifying detected failures according to predetermined failure types; counter means responsive to outputs of said failure type identification means for counting failures of each said predetermined types; failure address registers for storing the row or column address of first and last detected failures in a column or row under test; and a failure mask register for storing a failure mask containing results of comparisons of memory data outputs against expected data outputs; means responsive to phase input signals and memory access mode signals for selecting failure data to insert into said failure summary a failure summary transfer register having a bit length equal to or less

than the time required to test a column or row of said memory divided by the period of said second clock; and means for transferring said failure summary from said circuit via a circuit serial output under control of a second clock while testing the next column or row, if any, of a memory under test.